Claims

What is claimed is:

1. A signal path for linking a node of an electronic device to a terminal of an IC tester, the signal path comprising:

a probe for contacting said node; and

a conductive path for linking said probe to said terminal,

wherein said node, said terminal and said conductive path have impedances sized relative to one another to substantially optimize a frequency response characteristic of said signal path.

2. The signal path in accordance with claim 1 wherein said impedances include inductances in series with said signal path and capacitances shunting said signal path.

3. The signal path in accordance with claim 1 wherein said conductive path comprises:

a probe card including first conductors forming a first part of said conductive path;

a space transformer including second conductors forming a second part of said conductive path; and

an interposer including third conductors for conveying signals between said first and second conductors,

wherein said impedances include impedances of said node and of said first, second and third conductors.

4. The signal path in accordance with claim 1 wherein said frequency response characteristic is one of maximal passband width, maximal passband flatness and maximal passband power.

5. The signal path in accordance with claim 1 wherein said impedances are sized relative to one another so that said interconnect system forms a multiple-pole Butterworth filter.

6. The signal path in accordance with claim 1 wherein said impedances are sized relative to one another so that said interconnect system forms a multiple-pole Chebyshev filter.

7. A signal path for linking a node of an integrated circuit (IC) to a terminal of an IC tester, the signal path comprising:

a conductive pad implemented on said IC and linked to said node;

a probe for contacting said conductive pad; and

conductive means for linking said probe to said terminal,

wherein said conductive pad, said terminal and said conductive means have impedances sized relative to one another to substantially optimize a frequency response characteristic of said signal path.

8. The signal path in accordance with claim 7 wherein said impedances include inductances in series with said signal path and capacitances shunting said signal path.

9. The signal path in accordance with claim 7 wherein said conductive means includes a printed circuit board via having a capacitance that is one of said impedances.

10. The signal path in accordance with claim 7 wherein said conductive means includes a trace having a characteristic impedance that is one of said impedances.

11. The signal path in accordance with claim 7 wherein said conductive means includes a spring contact having an inductance that is one of said impedances.

12. The signal path in accordance with claim 7 wherein said conductive means comprises:

a printed circuit board via having a capacitance that is one of said impedances,

a trace having a characteristic impedance that is one of said impedances, and

a spring contact having an inductance that is one of said impedances,

13. The signal path in accordance with claim 7 wherein said conductive means comprises:

a probe card including first conductors forming a first part of said signal path;

a space transformer including second conductors forming a second part of said signal path; and

an interposer including a third conductor for conveying a signal between said first and second conductors,

wherein said impedances include impedances of said first, second and third conductors.

14. The signal path in accordance with claim 7 wherein said frequency response characteristic is one of maximal passband width, maximal passband flatness and maximal passband power.

15. The signal path in accordance with claim 7 wherein said impedances are sized relative to one another so that said interconnect system forms a multiple-pole Butterworth filter.

16. The signal path in accordance with claim 7 wherein said impedances are sized relative to one another so that said interconnect system forms a multiple-pole Chebyshev filter.

17. A method for sizing impedances of a signal path connecting a node of an integrated circuit (IC) to a terminal of an IC tester, wherein the signal path comprises a bond pad connected to said node, a probe contacting said bond pad, and conductive means linking said probe to said terminal, the method comprising the step of

adjusting impedances of said bond pad, said probe, and said conductive means relative to one another so as to optimize a characteristic of a frequency response of said signal path.

18. The method in accordance with claim 17 wherein said characteristic of said frequency response is one of maximal passband width, maximal passband flatness and maximal passband power.

19. The method in accordance with claim 17 wherein said impedances are adjusted such that said signal path acts substantially as a multiple-pole Butterworth filter.

20. The method in accordance with claim 17 wherein said impedances are adjusted such that said signal path acts substantially as a multiple-pole Chebyshev filter.